TrustNode

Eine hardware-beschleunigte Prototyping-Plattform für TSN

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InnoRoute

- Innovativer Technologietreiber aus München
- Beiträge zu zahlreichen Forschungsprojekten:
  - Greenet
  - Treufunk
  - CHARISMA-5G
  - SELFNET-5G
  - FlexSi-Pro
  - TacNet
  - TSN4KMU
- Kleine Teams mit großem Innovationspotential

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TrustNode Key-Features

Flexibel

- Neue Datenpfadfunktionen in Sekunden
- OpenSource Software mit großer Community
- FPGA-extends-software Konzept

Kompatibel

- Testing: LNI4.0 LABS NETWORK INDUSTRIE 4.0

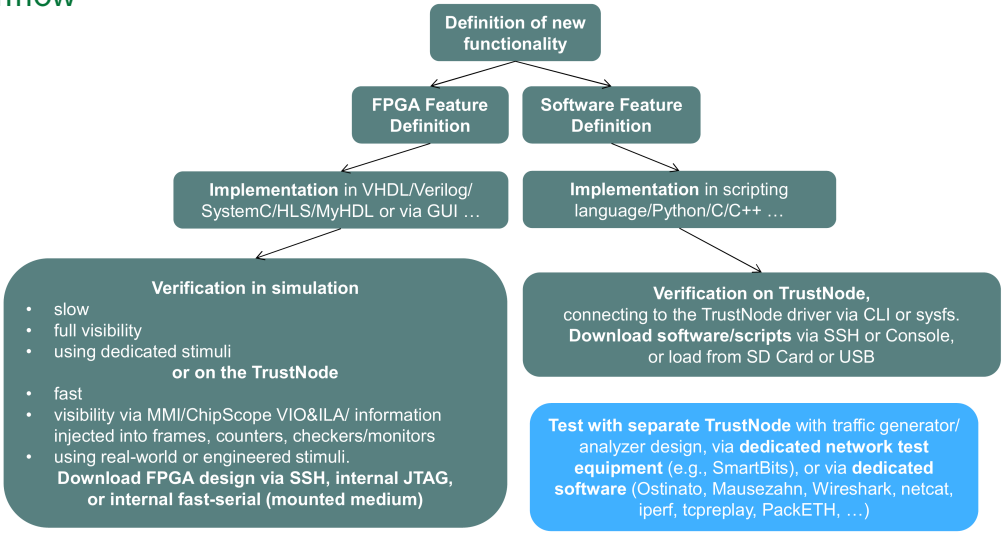
Innovative

- Laufende Förderprojekte generieren fortlaufend neue Features

Robust

- 19" Aluminium Gehäuse
- ESD Schutz für alle Interfaces (auch interne experimental pins)

Designflow


Definition of new functionality
FPGA Feature Definition
Software Feature Definition
Implementation in VHDL/Verilog/ SystemC/HLS/MyHDL or via GUI …
Implementation in scripting language/Python/C/C++ …
Verification in simulation
slow
full visibility
using dedicated stimuli
or on the TrustNode
fast
visibility via MMI/ChipScope VIO&ILA/ information injected into frames, counters, checkers/monitors
using real-world or engineered stimuli.
Download FPGA design via SSH, internal JTAG, or internal fast-serial (mounted medium)
Verification on TrustNode, connecting to the TrustNode driver via CLI or sysfs. Download software/scripts via SSH or Console, or load from SD Card or USB
Test with separate TrustNode with traffic generator/ analyzer design, via dedicated network test equipment (e.g., SmartBits), or via dedicated software (Ostinato, Mausezahn, Wireshark, netcat, iperf, tcpreplay, PackETH, …)

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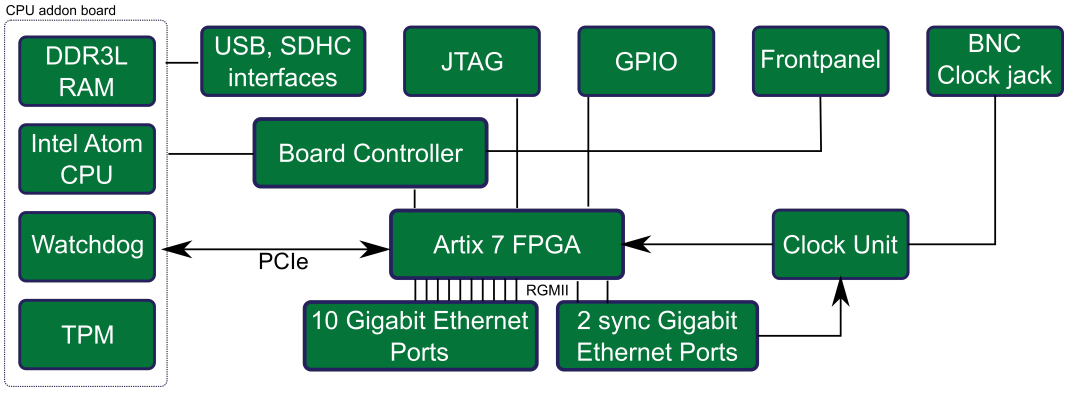
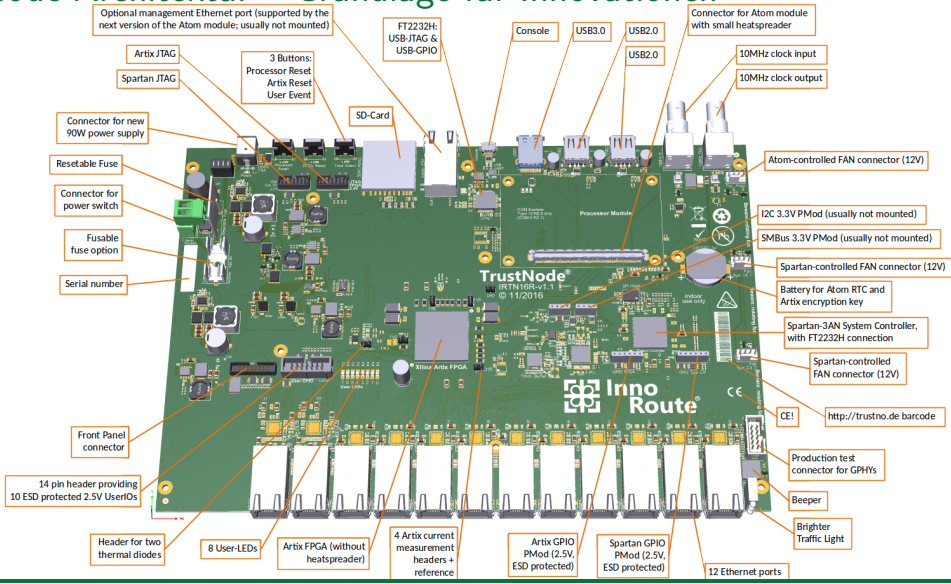
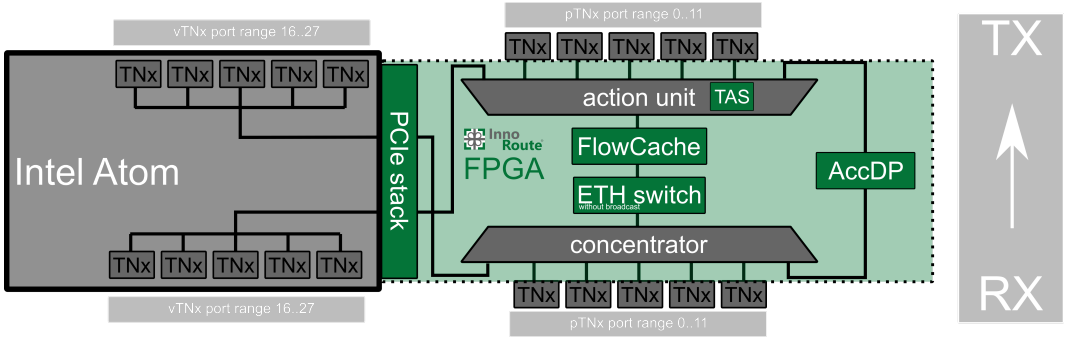
TrustNode Architektur – Grundlage für Innovationen



TrustNode Architektur – Grundlage für Innovationen

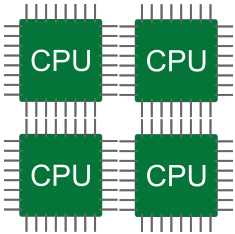


TrustNode Architektur



CPU-Subsystem Architektur

- Intel Atom E3845
- 4x1.9 GHz
- x86_64 Architektur
  - Auch für Desktop-OS wie Windows geeignet
  - Closedsource Software ist ohne crosscompiling lauffähig
- 4 GB RAM
- UEFI secure boot



Datenblatt: `https://www.intel.com/content/dam/www/public/us/en/documents/datasheets/atom-e3800-family-datasheet.pdf`

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Software features

- WEB-Oberfläche
- NetConf Interface
- OpenFlow Interface
- FPGA Programmierung
  - FTDI-JTAG
  - FTDI-optomode(schneller)
- FPGA Konfiguration über MMI
  - FlowCache (OpenFlow acceleration)
  - Acceleration DataPath
  - TSN Core
  - Weitere Konfiguration
- FPGA Konfiguration über CLI Software
  - FlowCache
  - Time Aware Shaper
  - Acceleration DataPath
  - 6Tree Routing [1]
- Ethernet Treiber für FPGA PCIe Interface
  - Standard Linux Ethernet Interface
  - PTP Hardware Clock Gerät
  - Interrupt Verarbeitung für MMI und PCIe

SDN/TSN Interfaces

- OpenvSwitch Endpunkt auf CPU
  - Python Schnittstelle für automatische Flow-acceleration im FlowCache
- Einfach anpassbare REST Interface Vorlagen vorhanden.
- Sysrepo: NetConf, RESTconf
- OPC-UA (comming soon)

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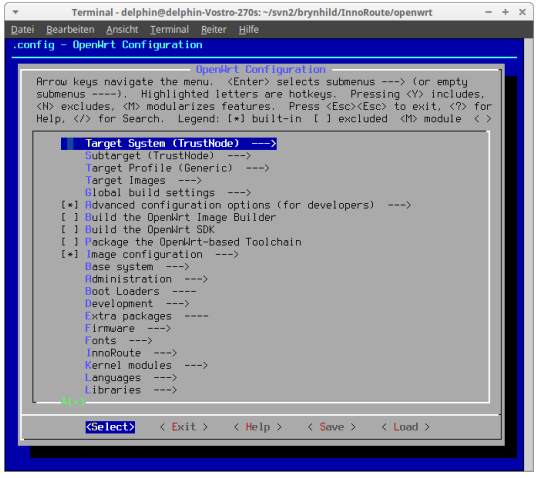
Folien: https://innoroute.com/i-tage/

TrustNode Software Entwicklungsumgebung

- OpenWRT BuildRoot-basierte Toolchain
  - Optimiert für embedded systems
  - Paketbasiert, einfach erweiterbar
  - Große & aktive Community mit InnoRoute als Gatekeeper
- Erstellt fertiges UEFI-Image mit Kernel und Root-Dateisystem
- Online verfügbar: `https://github.com/InnoRoute`



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FPGA Erweiterung

- Artix7 FPGA
- XILINX VIVADO
- InnoRoute VHDL-Lizenz

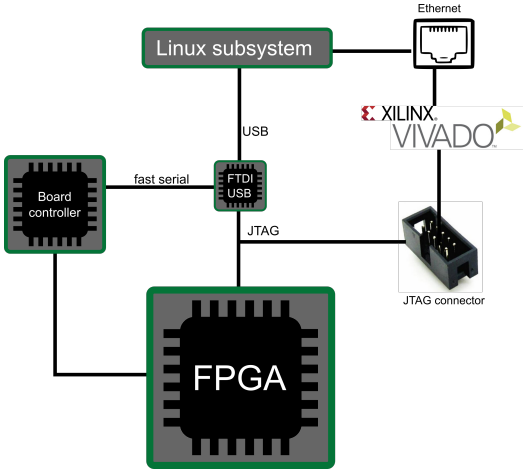

Figure: FPGA access

FPGA Modul Struktur

FIFO, SFD/FCS strip, NoC header creation, 64 Byte segmenting, segment interleaving

parsing, classification, set outputport

buffering, queuing, scheduling

packet modification (using NoC-information)

NoC-header stripping, SFD/FCS adding, timestamping

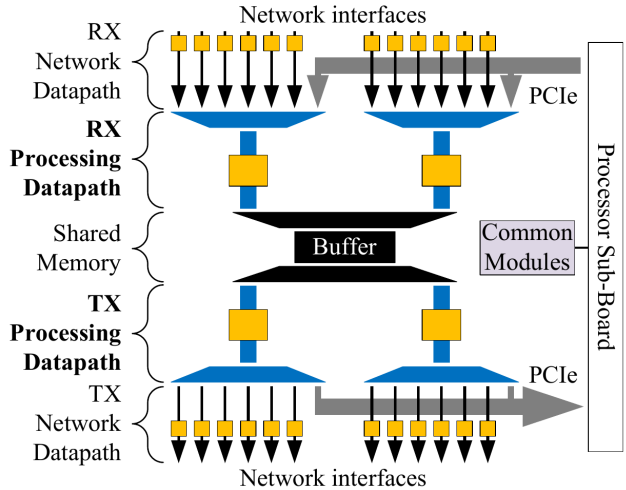

Figure: TrustNode Datenpfad Blöcke [2]

Datenpfad Module

- Pipeline Architektur mit Finite state machines (FSMs)
- Zugriff auf Memory Mapped Interface (MMI), oder andere Schnittstellen

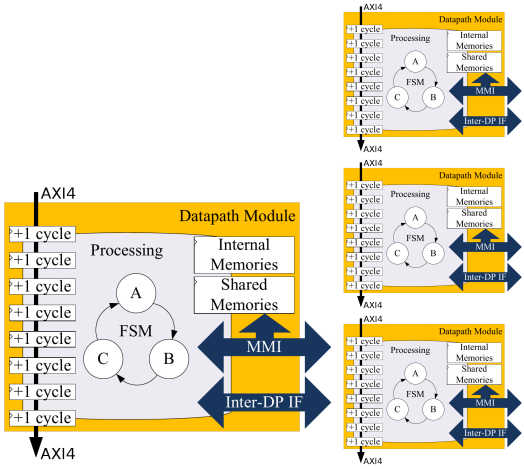

Figure: Funktionserweiterung durch modulare Block Verkettung. [2]

Kleine Latenz durch cut-through

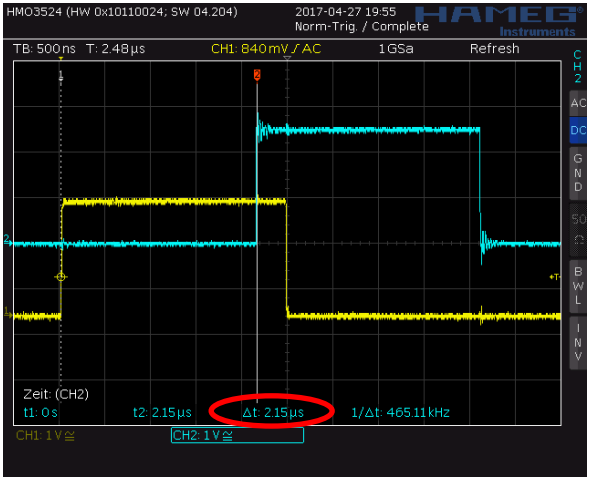

Figure: Delay von PHY zu PHY

Deterministische Latenz der Module

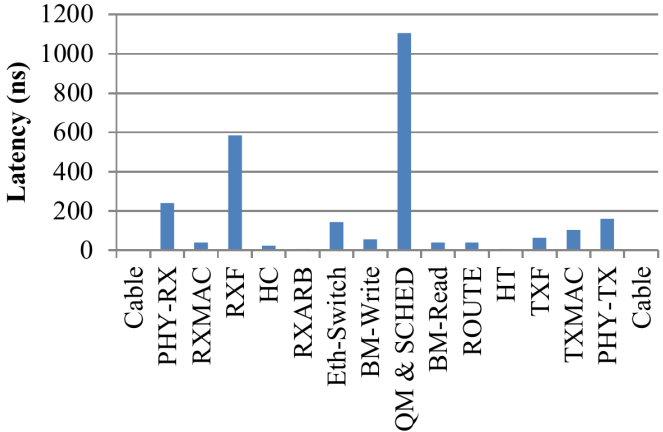

Figure: Latenz der Datenpfad Module [2]

Wenig Jitter

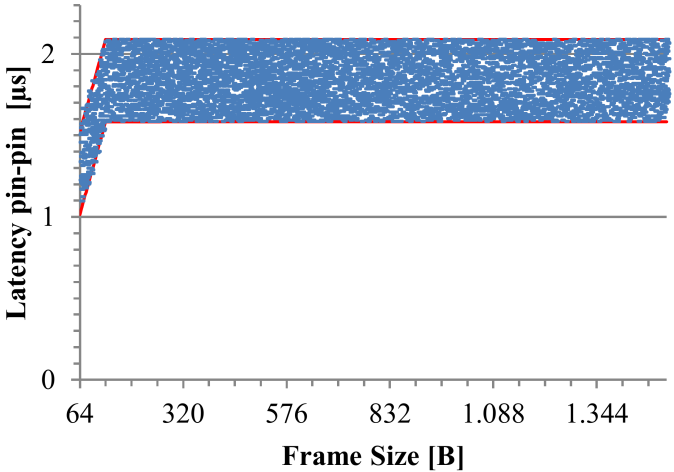

Figure: Jitter für verschiedene Framegrößen[2]

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TSN Experiment/Video

- Webinterface
- Open vSwitch
- FlowCache
- Time Aware Shaper

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Zusammenfassung: Flexibel, Innovativ, TSN ready, ...

- Hohe Flexibilität:
  - Programmierbare Hardware
  - Einfach erweiterbare OpenSource Software
- TSN ready
  - Precision Time Protocol (PTP)
  - Synchronous Ethernet (SyncE)
  - Time Aware Shaper (TAS)

- Unterstützte Standards:
  - IEEE 802.1 AS
  - IEEE 802.1 Qbv
  - (IEEE 802.1 Qcc) MSRP: work in progress
  - (IEEE 802.1 Qci) work in progress
- Standard Schnittstellen:
  - NetConf/RESTconf
  - OpenFlow
  - OPC-UA
  - ...

Order your TrustNode at

http://trustno.de

Questions?

Keep in touch! https://twitter.com/innoroutegmbh

https://de.linkedin.com/company/innoroute

Quellen I

A. Foglar, M. Parker, and T. Rokkas, *IPv6 source routing for ultralow latency draft-foglar-ipv6-ull-routing-04*, IETF Routing Area Working Group, Ed., 2018. [Online]. Available: https://tools.ietf.org/html/draft-foglar-ipv6-ull-routing-04.

C. Liß, M. Ulbricht, U. F. Zia, and H. Müller, "Architecture of a synchronized Low-Latency network node targeted to research and education," in *2017 IEEE 18th International Conference on High Performance Switching and Routing (HPSR) (IEEE HPSR'17)*, Campinas, Brazil, Jun. 2017.

Abkürzungen I

CLI Comand Line Interface

CPU Central Processing Unit

ESD Electrostatic Discharge

FSM Finite state machine

JTAG Joint Test Action Group

MSRP Multiple Stream Reservation Protocol

MMI Memory Mapped Interface

OVS Open vSwitch

PCIe Peripheral Component Interconnect Express

PHY Physical Layer Chip

Abkürzungen II

PTP Precision Time Protocol

REST Representational State Transfer

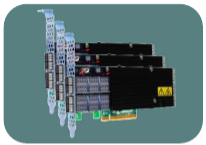
SyncE Synchronous Ethernet

TAS Time Aware Shaper

State of the Art

Dedicated **Switch/Router**

Missing control & visibility for custom functionality or high latency



PC with **FPGA cards optimized for low latency**

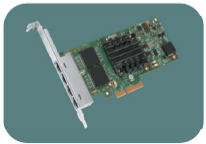
Few ports, only 10G+ interfaces.

Latency depends on software stack and input/output port combination.

PC with one or two **NetFPGA** cards

High latency (store & forward) and few ports.

No frequency synchronization option.



XEON **servers with standard NICs**

Easily available and scalable, but higher latency